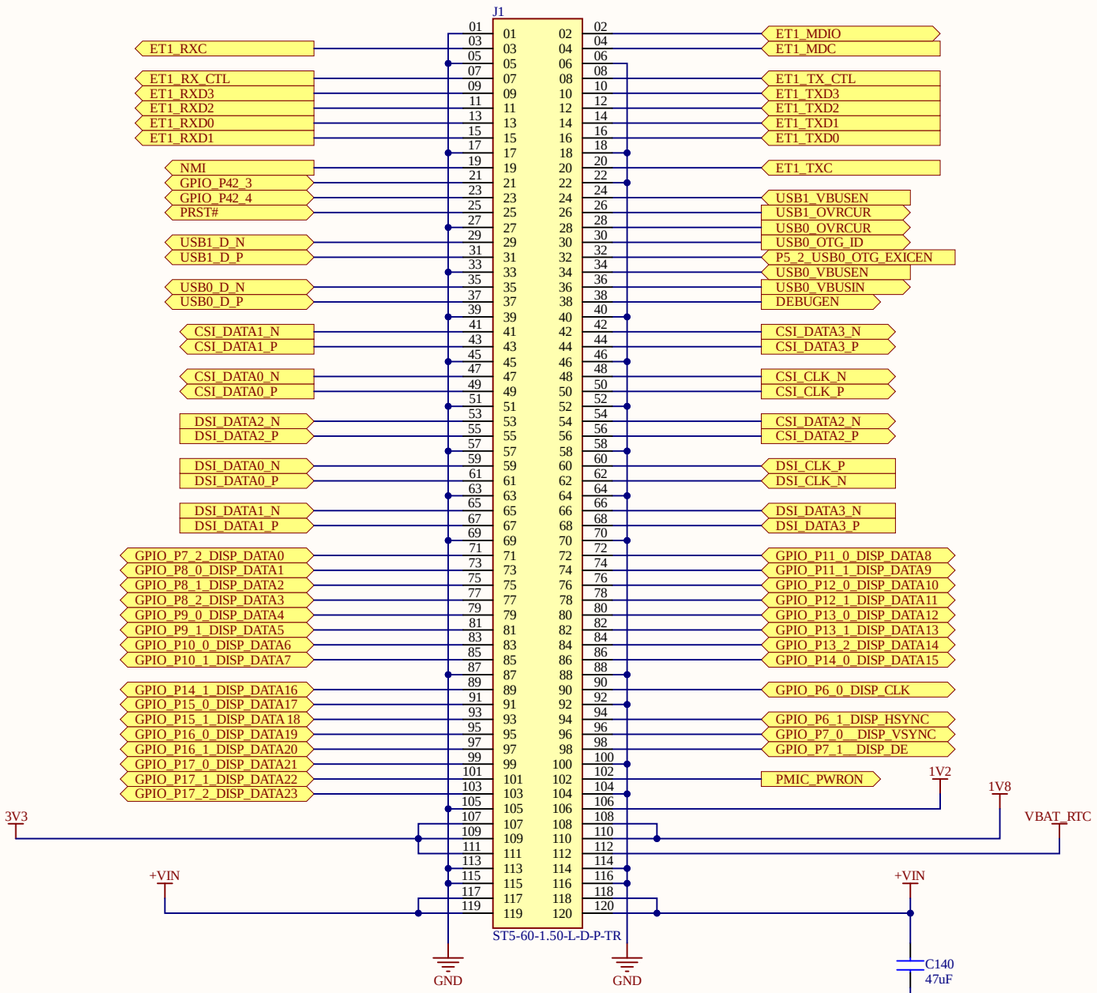

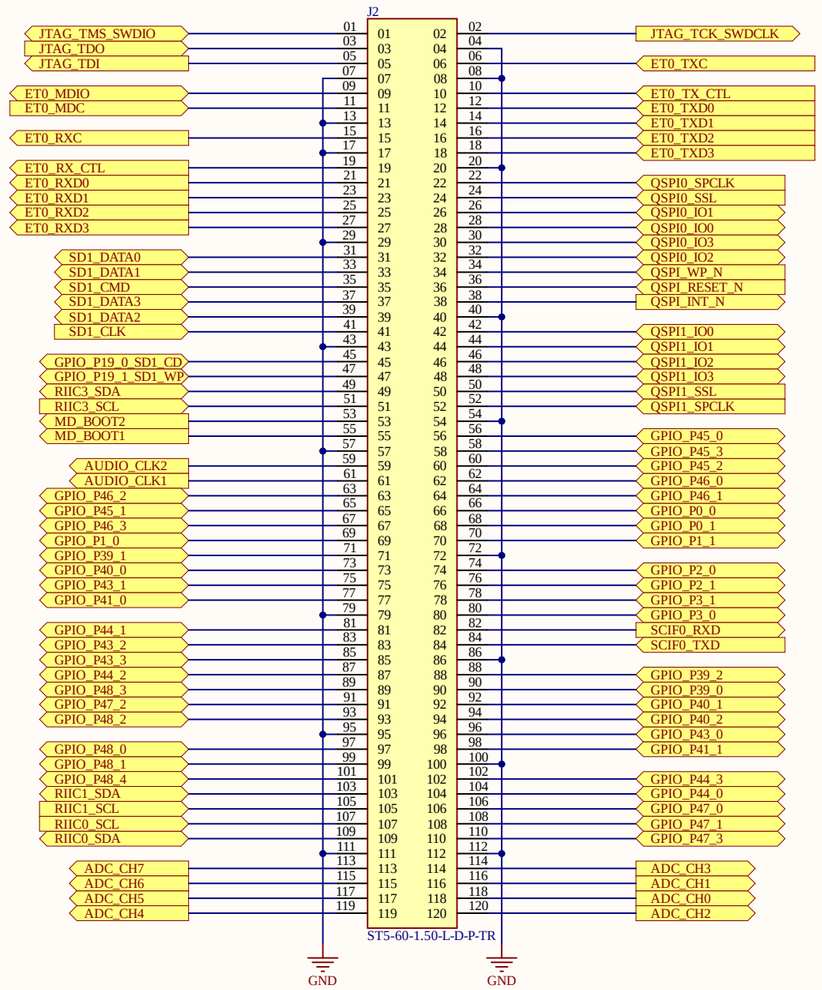

MH1
M2 NPTH 2.4mm drill with 4.5 mm clearance both sides

MH2
M2 NPTH 2.4mm drill with 4.5 mm clearance both sides

MH3
M2 NPTH 2.4mm drill with 4.5 mm clearance both sides

MH4
M2 NPTH 2.4mm drill with 4.5 mm clearance both sides

Top Side Fiducials

FID1 FID_1mm_3mm

FID2 FID_1mm_3mm

FID3 FID_1mm_3mm

Bottom Side Fiducials

FID4 FID_1mm_3mm

FID5 FID_1mm_3mm

FID6 FID_1mm_3mm

mistywest
554 E 15th Ave.
Vancouver, BC
V5T 2R5

DESIGNED BY		DWG TYPE	PCB SCHEMATIC
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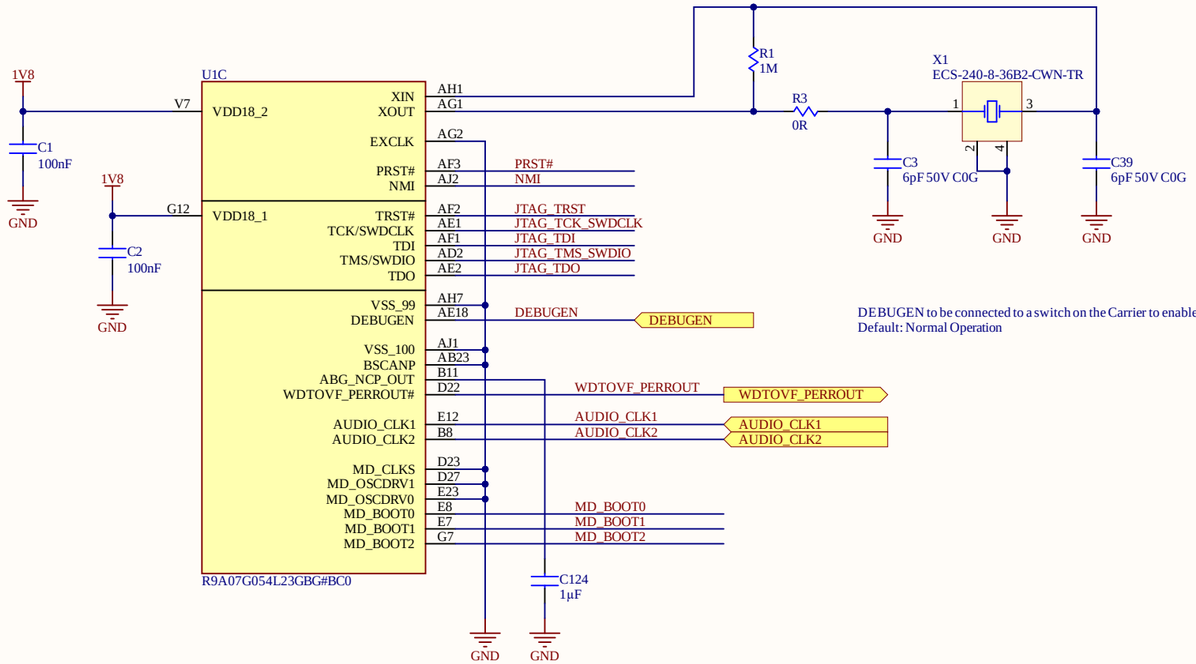
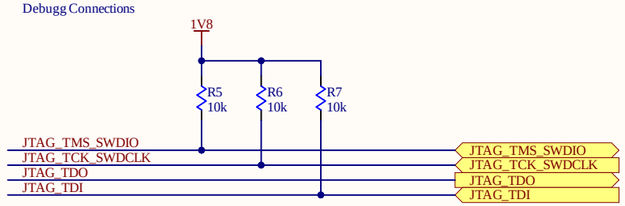
DATE	PCB #	SOM001	REV B SHT * OF *

AUDIO_CLK1 and AUDIO_CLK2 Require pull resistor on the Carrier when not in use!!!

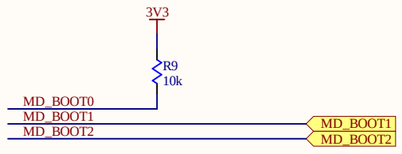


DEBUGEN to be connected to a switch on the Carrier to enable DEBUG mode
Default: Normal Operation

Debugg Connections



Boot Pins
Default Setup should be: 001 (1.8V eMMC)

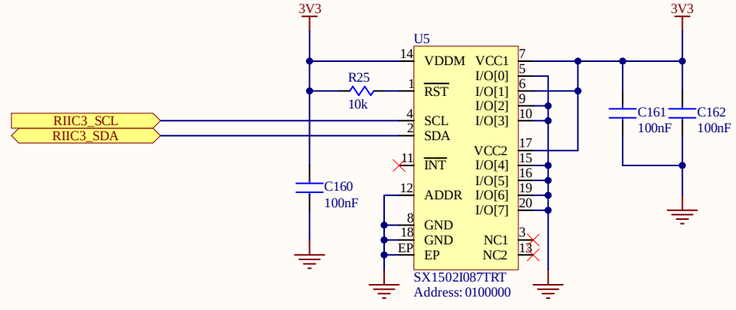


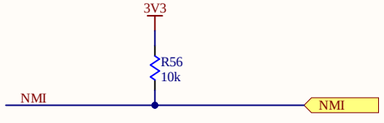
Pins directly connected to GND:

MD_OSC0	Renesas suggests connecting OSC0 and 1 pins to GND
MD_OSC1	
BSCANP	Background scan disabled
EXCLK	Crystal oscillator on CPU used
MDCLKS	SSCG for PLL3 off

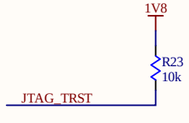
Boot Options (set on the Carrier):

	MD_BOOT2	MD_BOOT1
1.8V eMMC	0	0
1.8V QSPI FLASH	0	1
SCIF0	1	0





JTAG_TRST is not used for debugging and needs to be pulled up



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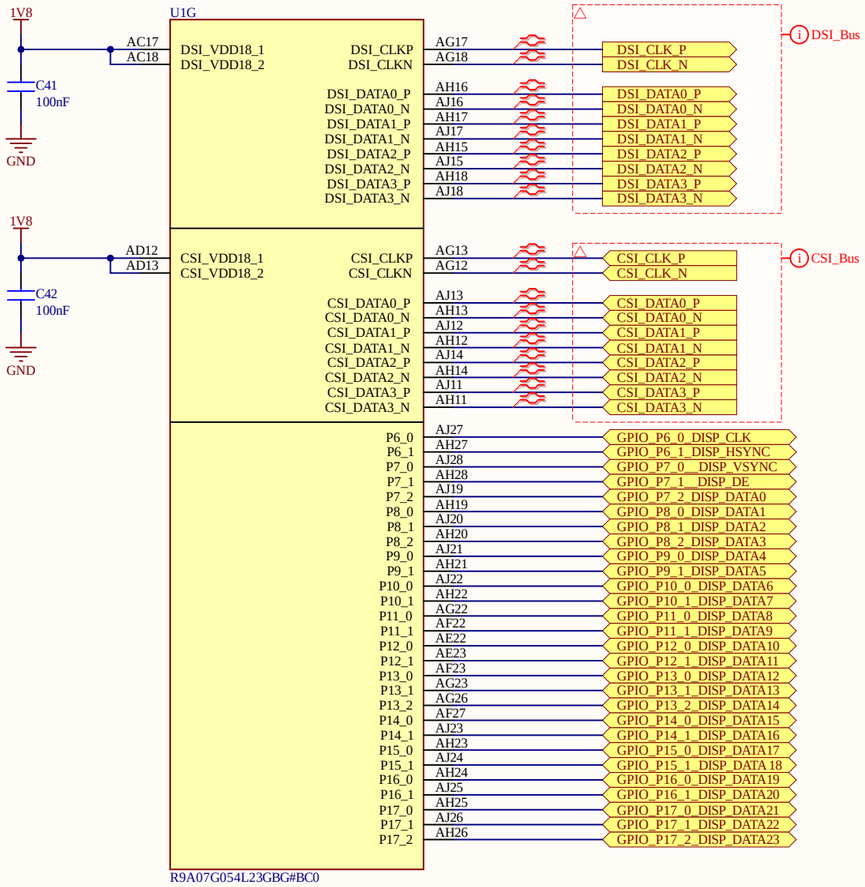
		DRAWN BY		PCB SCH.	Control.SchDoc
		APPROVED BY	Approved Name	PROJECT	
		DATE	2022-12-23	PCB #	SOM001
		REV	B	SHT	* OF *



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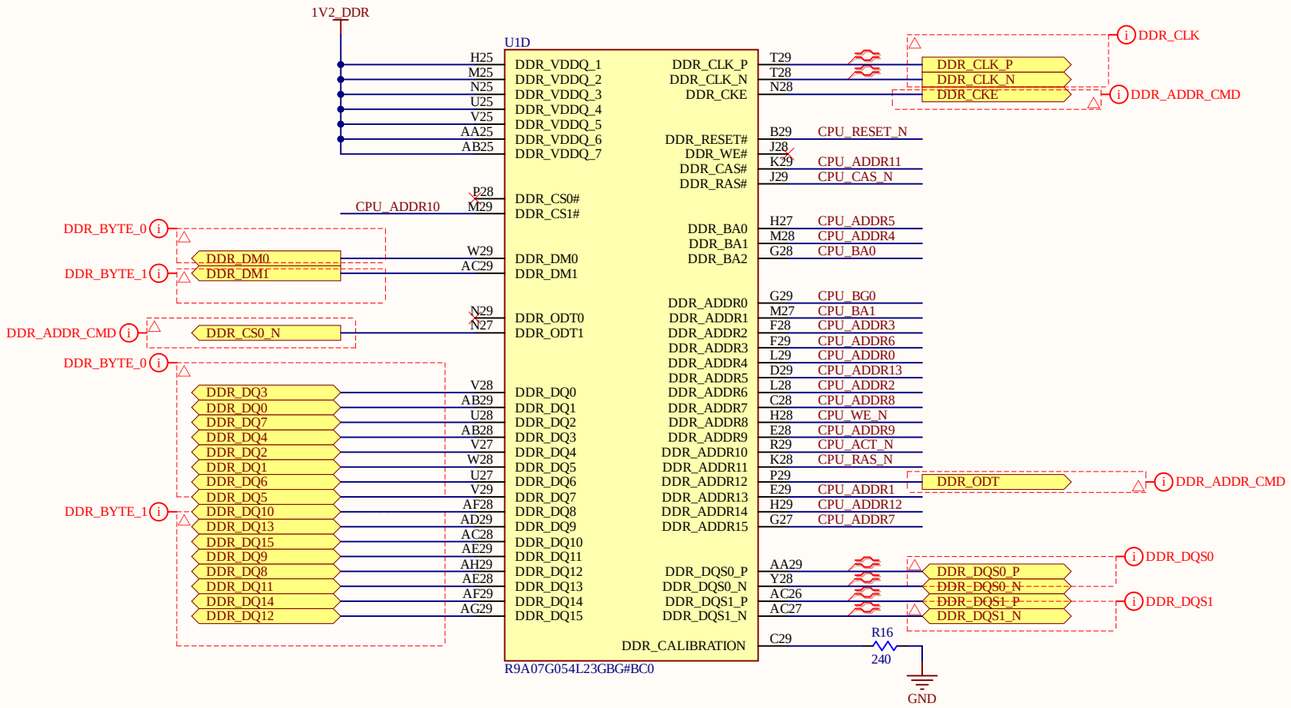
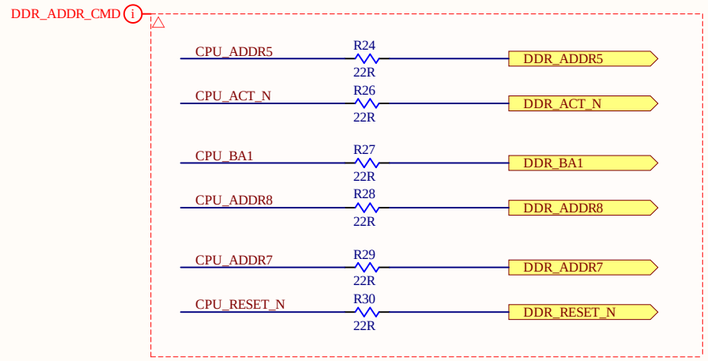
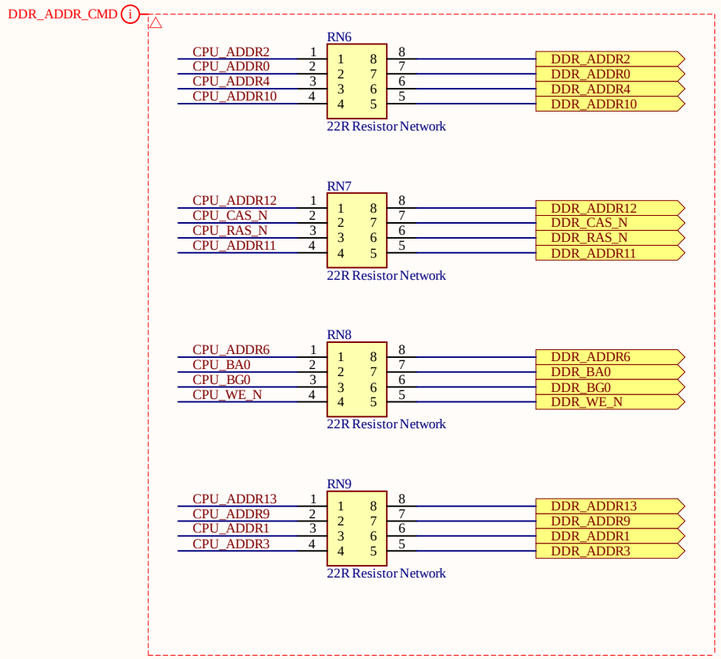
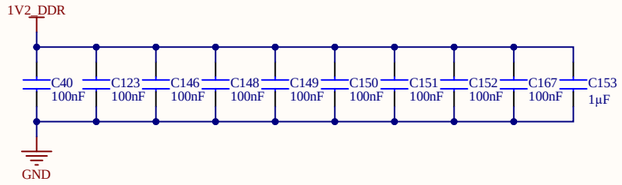
		DRAWN BY		PCB SCH.	CSI_DSI.SchDoc	
		APPROVED BY	Approved Name	PROJECT		
		DATE		PCB #	SOM001	REV B SHT * OF *









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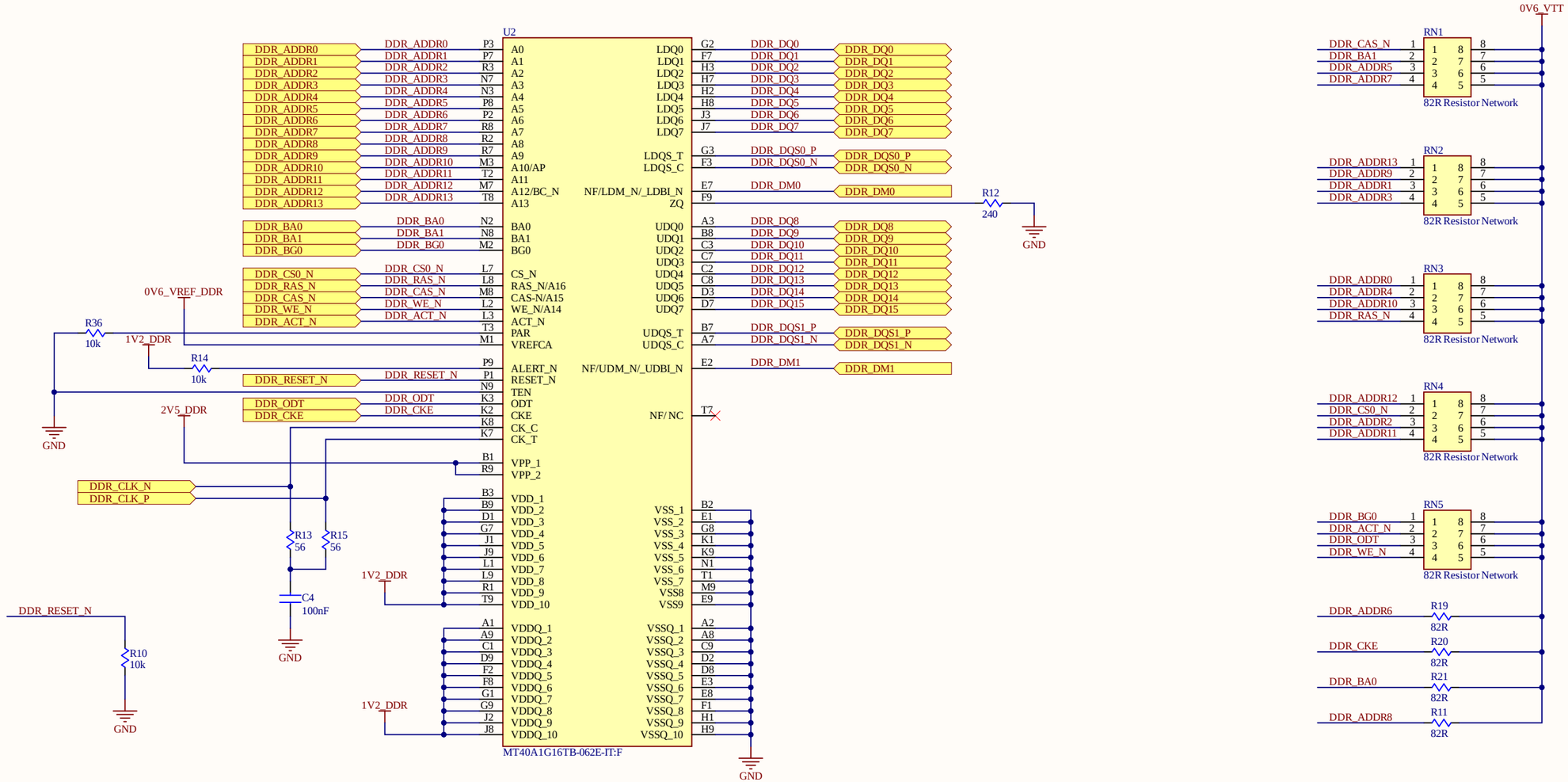
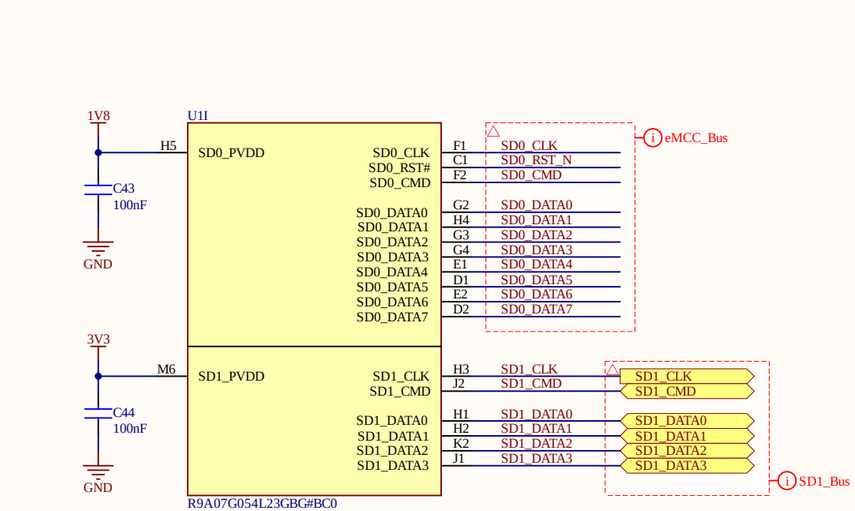
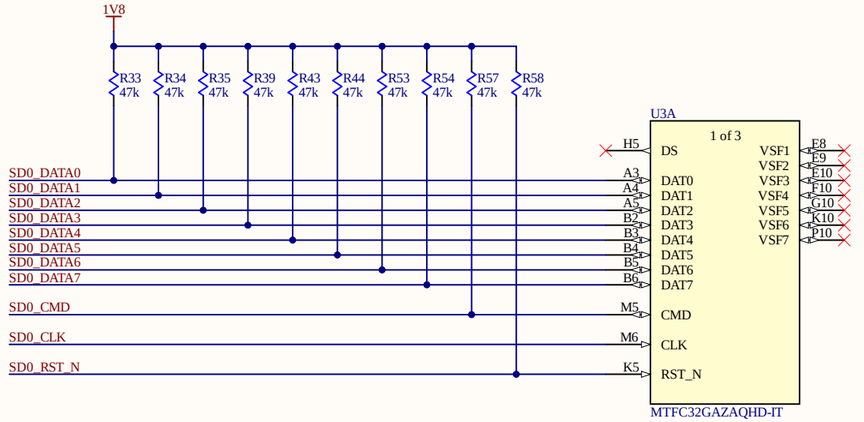
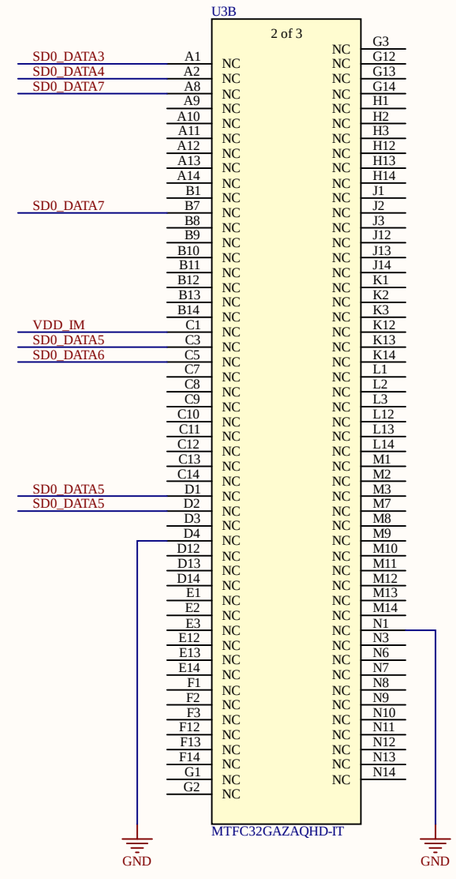
		DRAWN BY		PCB SCH.	DDR4_CPU.SchDoc
		APPROVED BY	Approved Name	PROJECT	
		DATE		PCB # SOM001	REV B SHT * OF *

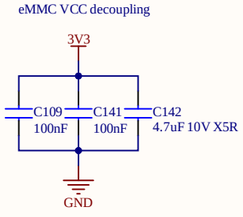


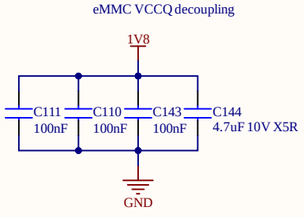
mistywest	554 E 15th Ave. Vancouver, BC V5T 2R5	DESIGNED BY		DWG TYPE	PCB SCHEMATIC
		DRAWN BY		PCB SCH.	DDR4_Memory.SchDoc
		APPROVED BY	Approved Name	PROJECT	
		DATE		PCB #	SOM001
		REV	B	SHT	* OF *

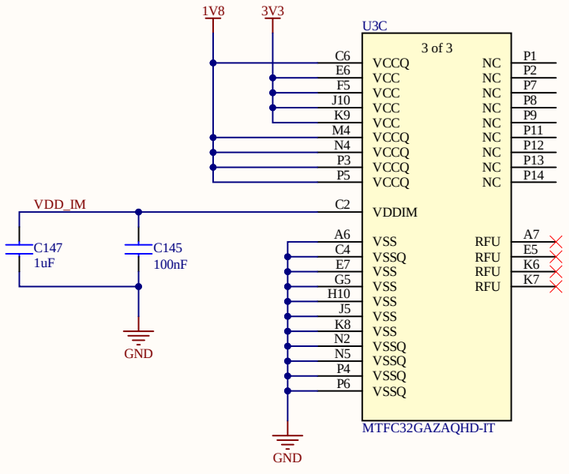

1V8
U1I
H5
SD0_PVDD
C43
100nF
GND
SD0_CLK
SD0_RST#
SD0_CMD
SD0_DATA0
SD0_DATA1
SD0_DATA2
SD0_DATA3
SD0_DATA4
SD0_DATA5
SD0_DATA6
SD0_DATA7
F1 SD0_CLK
C1 SD0_RST_N
F2 SD0_CMD
G2 SD0_DATA0
H4 SD0_DATA1
G3 SD0_DATA2
G4 SD0_DATA3
E1 SD0_DATA4
D1 SD0_DATA5
E2 SD0_DATA6
D2 SD0_DATA7
eMCC_Bus
3V3
M6
SD1_PVDD
C44
100nF
GND
SD1_CLK
SD1_CMD
SD1_DATA0
SD1_DATA1
SD1_DATA2
SD1_DATA3
H3 SD1_CLK
J2 SD1_CMD
H1 SD1_DATA0
H2 SD1_DATA1
K2 SD1_DATA2
J1 SD1_DATA3
SD1_Bus
R9A07G054L23GBG#BC0

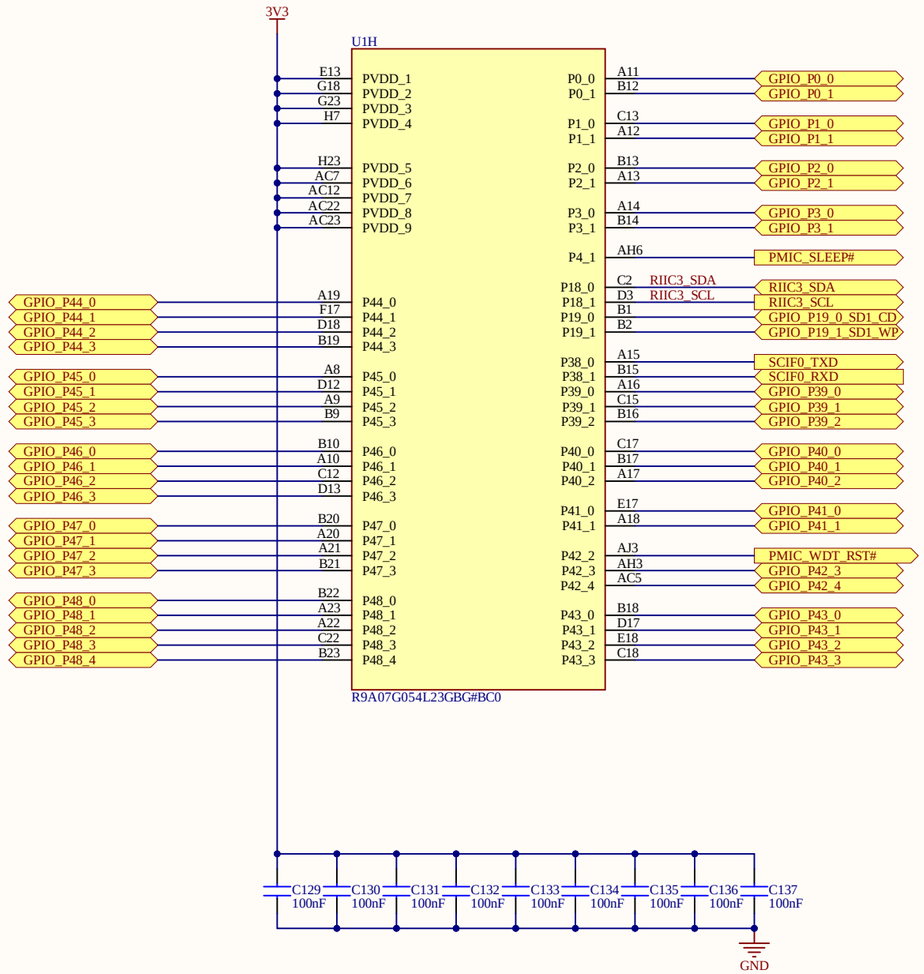

1V8
R33 47k
R34 47k
R35 47k
R39 47k
R43 47k
R44 47k
R53 47k
R54 47k
R57 47k
R58 47k
SD0_DATA0
SD0_DATA1
SD0_DATA2
SD0_DATA3
SD0_DATA4
SD0_DATA5
SD0_DATA6
SD0_DATA7
SD0_CMD
SD0_CLK
SD0_RST_N
U3A
1 of 3
H5 DS
A3 DAT0
A4 DAT1
A5 DAT2
B7 DAT3
B3 DAT4
B4 DAT5
B5 DAT6
B6 DAT7
M5 CMD
M6 CLK
K5 RST_N
VSF1 E8
VSF2 E9
VSF3 E10
VSF4 F10
VSF5 G10
VSF6 K10
VSF7 P10
MTFC32GAZAQHD-IT

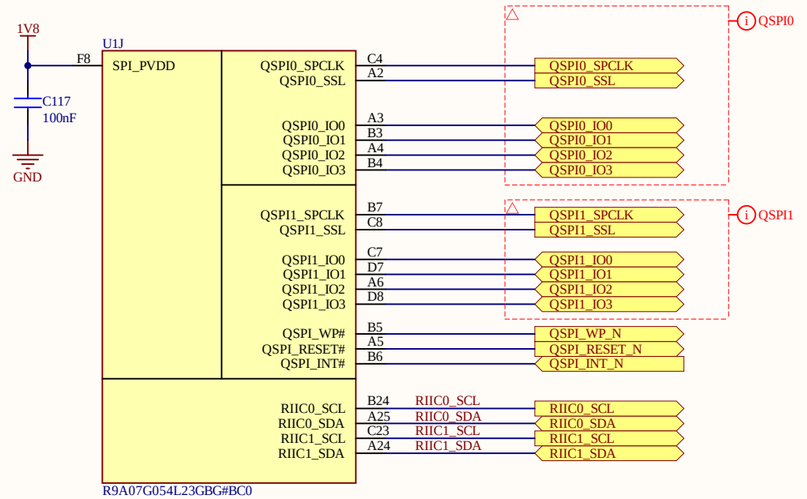

U3B
2 of 3
SD0_DATA3 A1
SD0_DATA4 A2
SD0_DATA7 A8
SD0_DATA7 B7
VDD_IM C1
SD0_DATA5 C3
SD0_DATA6 C5
SD0_DATA5 D1
SD0_DATA5 D2
NC
G3 G12 G13 G14 H1 H2 H3 H12 H13 H14 J1 J2 J3 J12 J13 J14 K1 K2 K3 K12 K13 K14 L1 L2 L3 L12 L13 L14 M1 M2 M3 M7 M8 M9 M10 M11 M12 M13 M14 N1 N3 N6 N7 N8 N9 N10 N11 N12 N13 N14
MTFC32GAZAQHD-IT
GND
GND

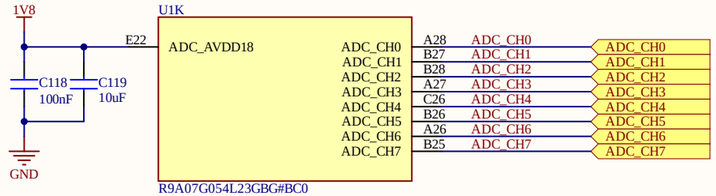

eMMC VCC decoupling
3V3
C109 100nF
C141 100nF
C142 4.7uF 10V X5R
GND

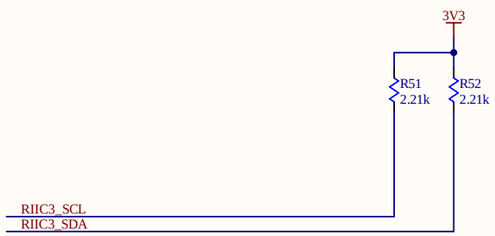

eMMC VCCQ decoupling
1V8
C111 100nF
C110 100nF
C143 100nF
C144 4.7uF 10V X5R
GND


1V8
3V3
U3C
3 of 3
C6 VCCQ
E6 VCC
F5 VCC
J10 VCC
K9 VCC
M4 VCCQ
N4 VCCQ
P3 VCCQ
P5 VCCQ
C2 VDDIM
A6 VSS
C4 VSSQ
E7 VSS
G5 VSS
H10 VSS
J5 VSS
K8 VSS
N2 VSSQ
N5 VSSQ
P4 VSSQ
P6 VSSQ
NC P1 P2 P7 P8 P9 P11 P12 P13 P14
RFU A7 E5 K6 K7
VDD_IM
C147 1uF
C145 100nF
GND
GND
MTFC32GAZAQHD-IT









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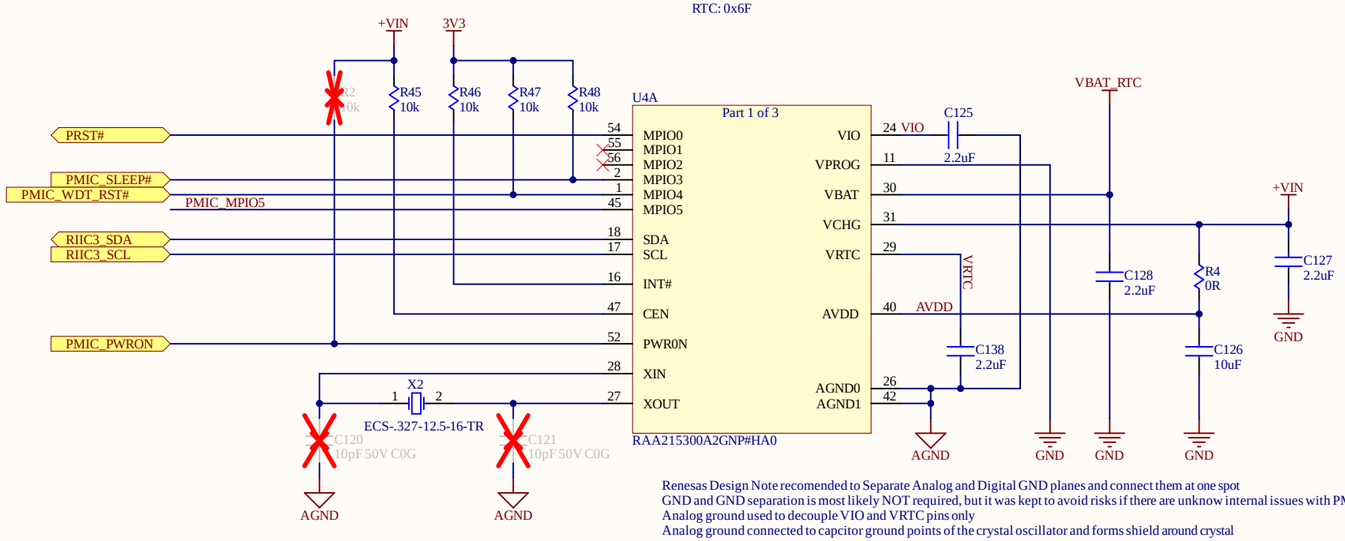
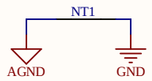
		DRAWN BY	PCB SCH.: GPIO_QSPI_ADC.SchDoc
		APPROVED BY: Approved Name	PROJECT
		DATE	PCB #: SOM001 REV: B SHT * OF *

PMIC I2C Addresses:
Main: 0x12
RTC: 0x6F

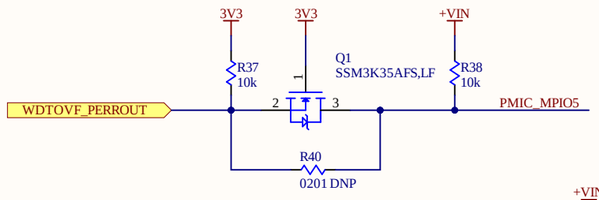


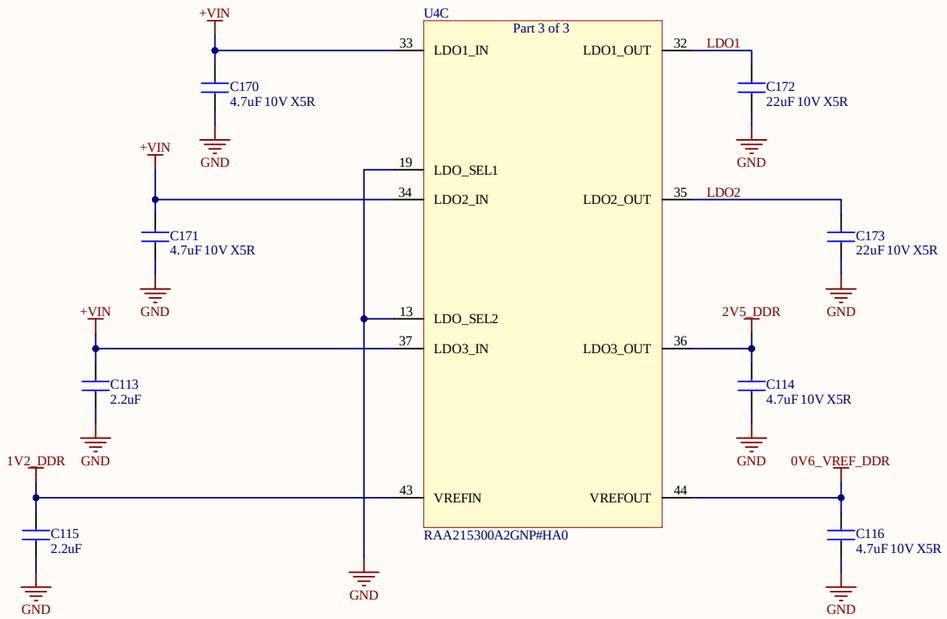
Renesas Design Note recomended to Separate Analog and Digital GND planes and connect them at one spot
GND and GND separation is most likely NOT required, but it was kept to avoid risks if there are unknow internal issues with PMIC
Analog ground used to decouple VIO and VRTC pins only
Analog ground connected to capcitor ground points of the crystal oscillator and forms shield around crystal

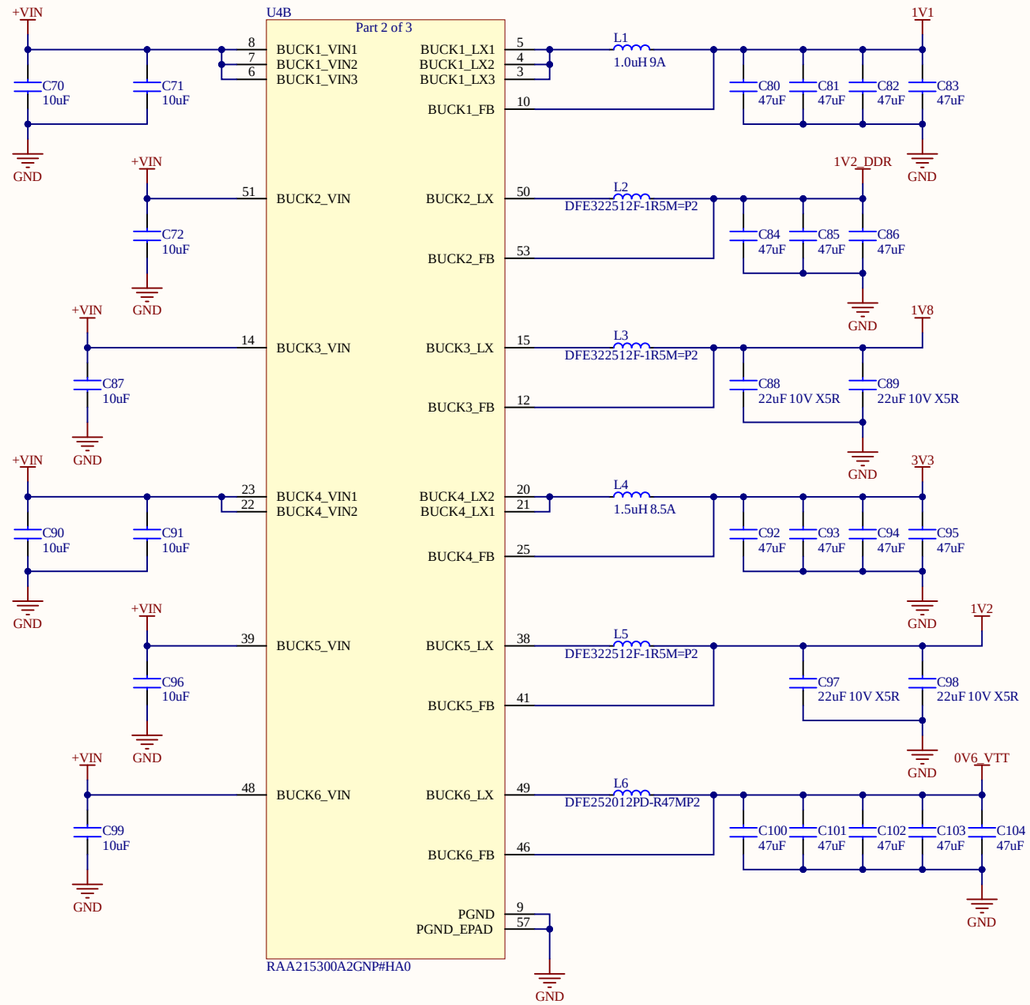
Net tie connecting AGND and GND



CPU WDT output to PMIC MPIO5 pin connection.
CPU pin should NOT be pulled to 5V: DO NOT populate both R40 and R38
WDTOVF_PERROUT is listed as High during reset so pull up most likely not required







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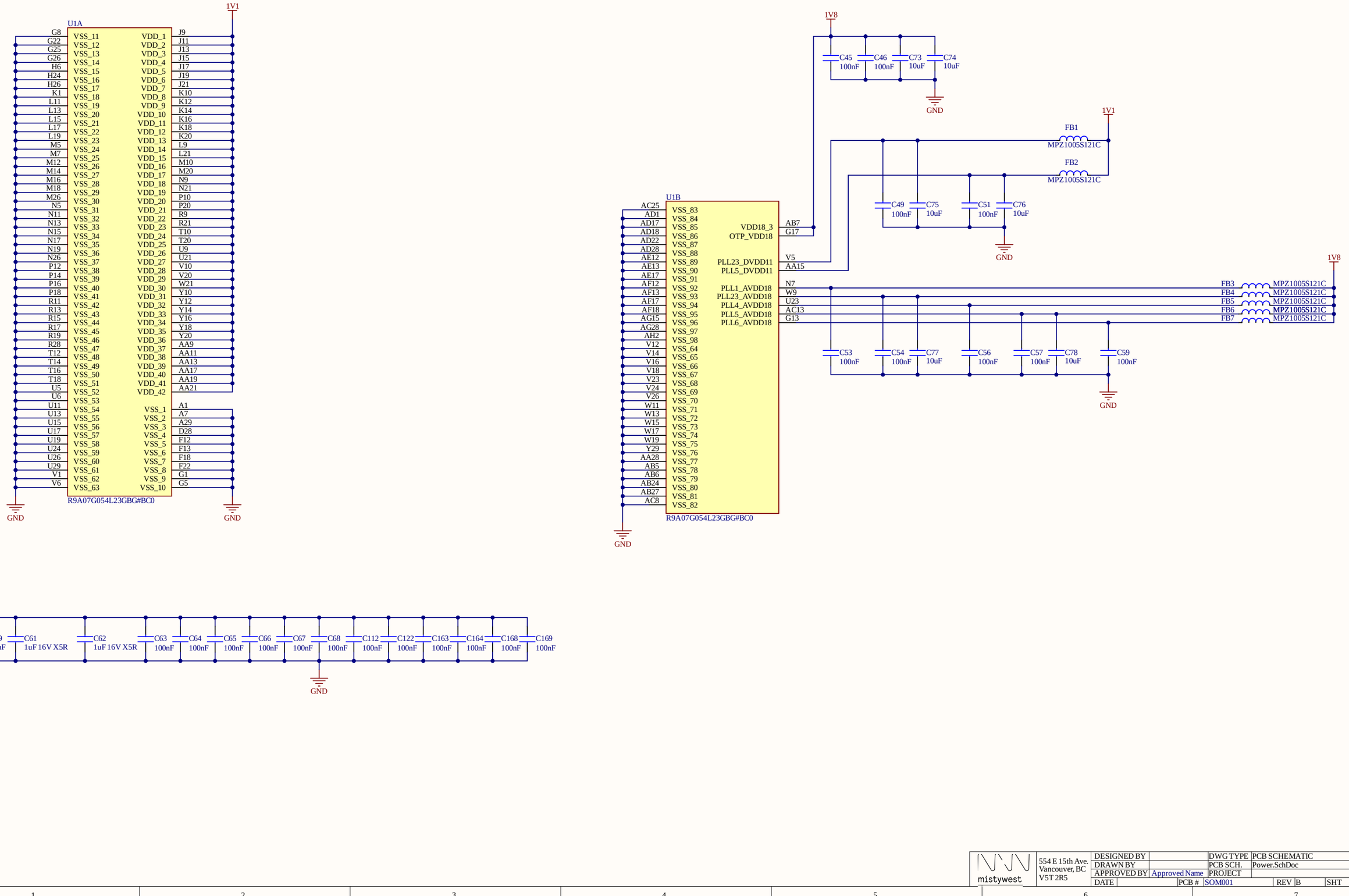
DESIGNED BY		DWG TYPE	PCB SCHEMATIC
DRAWN BY		PCB SCH.	PMIC.SchDoc
APPROVED BY	Approved Name	PROJECT	
DATE		PCB #	SOM001

REV B
SHT * OF *



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		DRAWN BY	PCB SCH.: Power.SchDoc
		APPROVED BY: Approved Name	PROJECT:
		DATE	PCB #: SOM001 REV: B SHT * OF *

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MW Logo New

Revision	Changes Since Last Revision
A	New Release
B	Added LDO1 and LDO2 circuits to PMIC Changed revision setup on U5 to 000 0010

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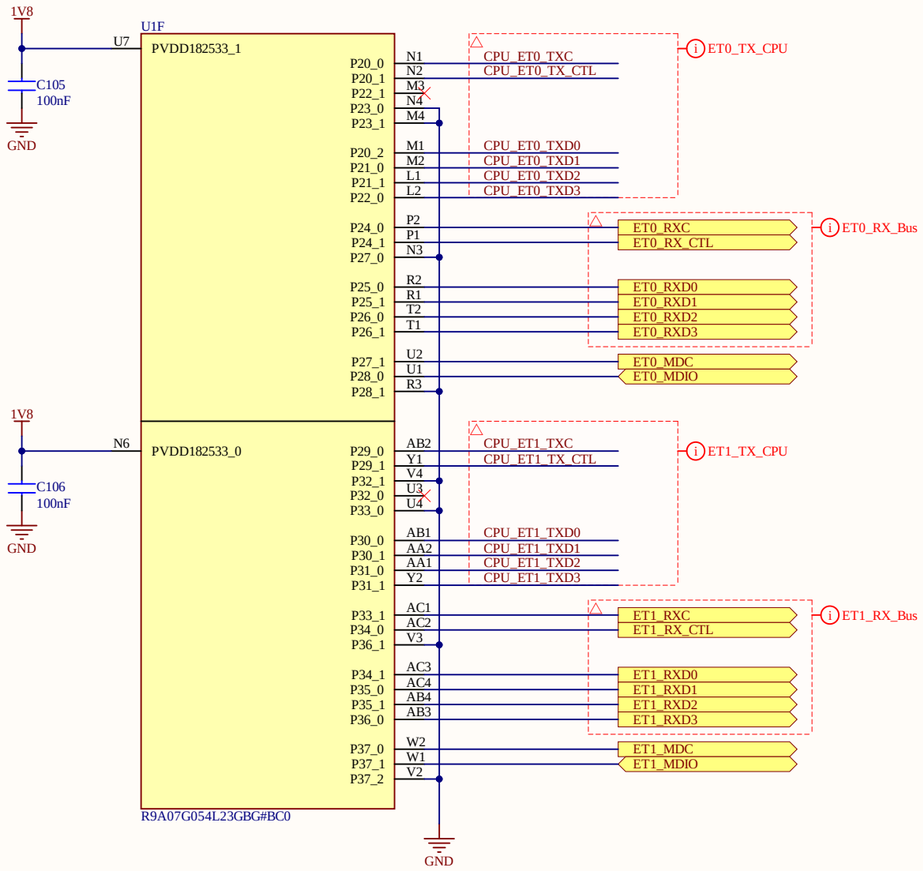
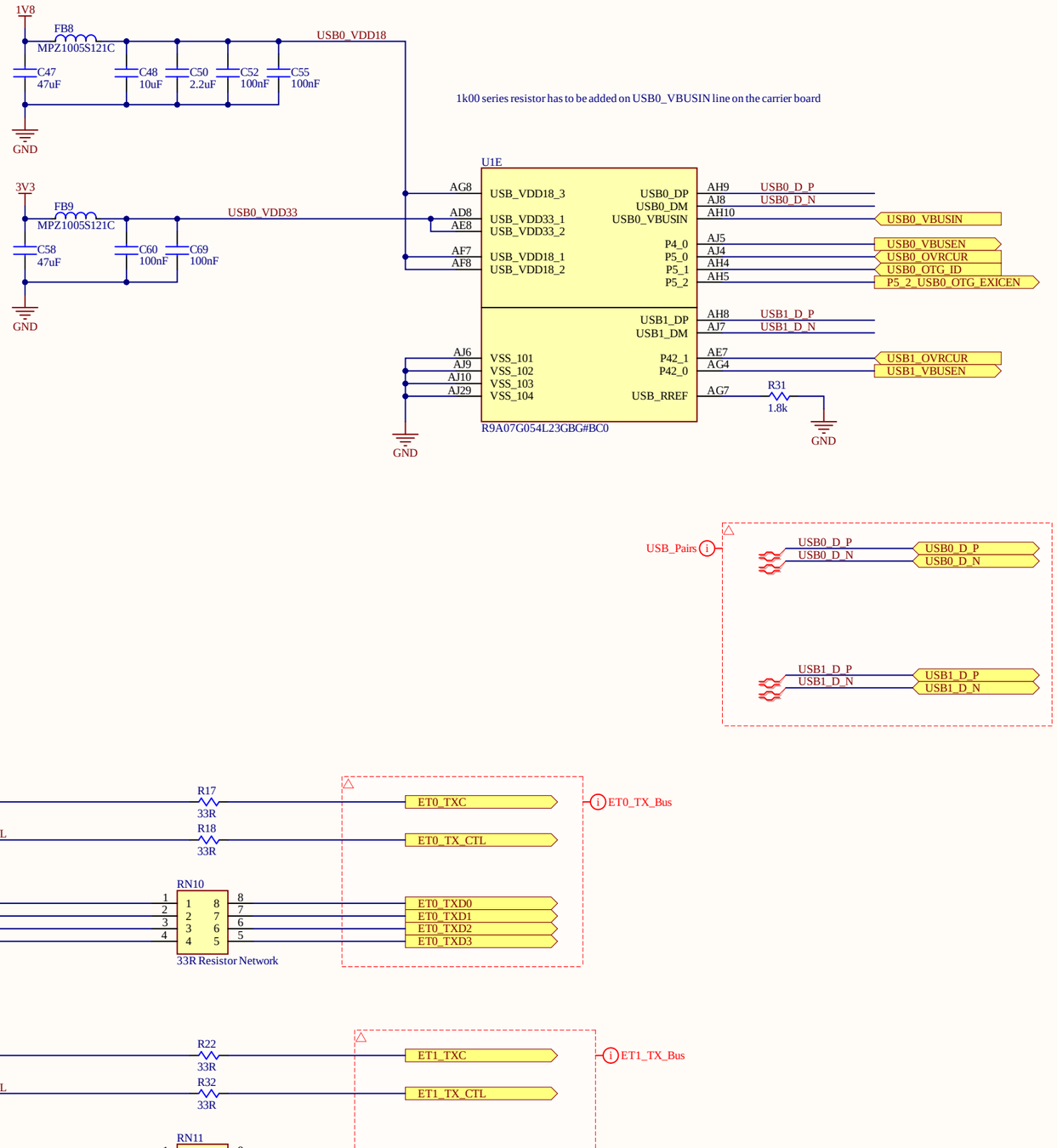
APPROVED BY	Approved Name	PROJECT	
DATE	PCB #	SOM001	REV B SHT * OF *





Verify if this is necessary!!!

Based on feedback from Renesas the following pins are grounded on both ETH0 and ETH1:
TX_COL
TX_CRS
RX_ERR
LINKSTA

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		DRAWN BY		PCB SCH.	USB_Ethernet.SchDoc
		APPROVED BY	Approved Name	PROJECT	
		DATE	PCB #	SOM001	REV B SHT * OF *